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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,448	11/25/2003	Astrid Elbe	S0193.0010	5966

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
09/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,448	ELBE ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-8* is/are pending in the application.

4a) Of the above claim(s) *9 and 11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/02/04,07/22/05,09/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-3,5-8 are examined on the merit of restriction requirement.

2. Claims 9,11-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/21/07.

Claims 5,6 objected to because of the following informalities: The use of language "is designed". It seems that the claimed invention is directed to the design, not the real implementation or a machine , or the like. Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye et al. (6,523,102) in view of O'Connor et al. (6,026,485).

4. As to claim 1, Dye taught at least :

a) a processor (see fig.4b [100] [200] [300]) having: an arithmetic unit for processing operands;

b) a register memory (main memory RAM, col.15, lines 3-15, system memory 200 in fig.4b) for storing operands; and

c) a register memory configuration unit designed to configure the register memory such that memory space in the register memory is assigned to operands (see also col.6, lines 38-65 for the virtual memory manager 620 to determine the allocation of compressed cache page) ;

d) a volatile external working memory (500, col.15, lines 3-10, see also memory modules DIMM, SIMM, SDDIMMs and RIMMs in col.14, lines 54-67, col.15, lines 1-12, see also the single memory chip 250 on driver 550 in col.18, lines 51-65 for

c) the register memory space being physically disposed within the processor (see main memory in the processor) , wherein at least a part of the resister memory space was mapped into the working memory (see allocated compressed cache page 240 in col.19, lines 40-67, col.20, lines 1-19), and
e) an address unit operable to address the resister memory space being physically disposed within the processor in the same way as the external working memory being physically disposed outside the processor (see the reallocation of active pages in col.19, lines 40-67, col.20, lines 1-19; pages are memory addresses ranges or locations).

5. As to the crypto coprocessor, Dye did not explicitly show the crypto coprocessor as claimed. However, Dye , in the same patent, taught his memory was used for encryption and decryption of in-memory system acceleration (col.19, lines 30-35). Since no specific structure of crypto coprocessor has been reflected in the claim, examiner holds that one or ordinary skill in the art should be able to use crypto processor in general into Dye, or the like, as it had been already suggested by Dye.

6. Dye did not specifically show that memory space in his register memory that was not assigned to operands was made available for data other than the operands as claimed. However, O'Connor taught a memory space in a register memory that was not assigned to operands was made available for other data than the operands (see fig.4C stack management unit, see also the constant pool [814] of local variables space in fig.8, see also fig.11 for the operands to the execution unit, see detail of operand memory stack region in fig.8, [812][813]). It would have been obvious to one of ordinary skill in the art to use O'Connor in Dye for including a memory space in a register memory that was not assigned to operands was made available for data other than the operands as claimed because the use of O'Connor could provide Dye the capability to adapt to particular requirements of the storage capacity at a predefined set of address space, and since Dye already taught the amount of memory space could be dynamically determined (col.19, lines 52-65), one of ordinary skill in the art should be

able to recognize the O'Connor memory space which was not being used by operands could be applicable into Dye for purpose of dynamic allocating of the memory space based on whether the memory space was used or not, and one of ordinary skill in the art should be able to recognize the potential use of memory space not used by operands (such as O'Connor's) into adjustable amount of memory space taught by Dye, or the like system.

7. For external memory , see Dye's fig.6. See also O'Connor's external memory in fig.1 .

8. As to claim 2, Dye also included single chip 250 on driver 550 in col.18, lines 51-65. See also O'Connor's included a single chip (see Internet chip in col.8, lines 8-15).

9. As to claim 5, O'Connor also included algorithm (see size defined in the program long in col.41, lines 35-40) for maximum length and algorithm (see size defined short in co1.41, lines 35-40) smaller length.

10. As to claim 6, see the encryption in col.2, lines 49-57.

11. As to claim 7,see Dye's internal connection in fig.6. See also O'Connor's internal bus in fig.1.

12. As to claim 8, O'Connor also configured the register memory in different length as needed (see the single word entry and double word entries I col.42, lines 36-67, col.43, lines 1-1-2).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Seysen (5,887,064) is cited for the teaching of crypto processor with the mapping external memory (see col.3, lines 24-53).

b) Carter et al. (5,909,540) is cited for the teaching of tracking memory space mapped to a volatile memory (see col.8, lines 24-35).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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GROUP